REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event, places the application in better condition for consideration on appeal, entry thereof is respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 31 to positively recite that the semiconductor layer includes a *residual porous layer*. Support for this amendment to Claim 31 is found at Page 10, lines 10-11 of the originally filed specification as well as in FIG. 2J whereat reference numeral 120' denotes the residual porous layer.

In addition to amending Claim 31, applicants have cancelled Claim 32 herein.

Since the above amendment to Claim 31 is fully supported by the specification of the instant application, entry thereof is respectfully requested. Applicants respectfully submit that the above amendment to Claim 31 does not raise any new issues that would require further consideration and/or searching on part of the Examiner since it provides a further feature to Claim 31 that was present in originally filed Claim 32.

In the present Office Action, Claims 31, 32, 35, 36 and 38 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent Application Publication No. 2002/000242 A1 to Matushiita, et al. ("Matushiita, et al."). Claims 37 and 40 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Matushiita, et al. and U.S. Patent No. 6,100,166 to Sakaguchi, et al. ("Sakaguchi, et al."). Claim 34 is rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Matushiita, et al. and U.S. Patent No. 6,350,945 to Mizuno ("Mizuno").

Concerning the § 102(e) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Matushiita, et al. since the applied reference does not disclose applicants' claimed structure recited in amended Claim 31. Specifically, Matushiita, et al. do not disclose an integrated circuit that includes a substrate selected from the group consisting of single crystal silicon, diamond, quartz, crystalline oxides, crystalline or amorphous nitrides, amorphous or glassy oxides, and organic-inorganic composites, an adhesive layer over said substrate, and a semiconductor layer including *a residual porous layer* on said adhesive layer, said semiconductor layer comprising at least one semiconductor device in said semiconductor layer, said semiconductor device formed in said semiconductor layer prior to bonding said semiconductor layer to the said adhesive layer and is selected from the group consisting of digital devices, analog devices, n-type metal-oxide-semiconductor devices (NMOS), p-type MOS (PMOS) devices, complementary MOS (CMOS) devices, bipolar transistors, bipolar and CMOS (BiCMOS) devices, SiGe bipolar or field effect devices, integrated passive devices,

Micro Electro Mechanical devices, voltage control oscillators, upconverters and downconverters.

Matushiita, et al. provide a method of forming a thin-film semiconductor device such as a thin film single-crystal solar cell which includes an upper plastic substrate 170 that is fixed to a first surface of a semiconductor layer 120 that includes components of a solar cell 140, 150 and 160 via an adhesion layer 171. The opposite surface of the semiconductor layer is fixed to a lower plastic layer 173 by an adhesive layer 172. Applicants observe that in Matushiita, et al. (see paragraph [0085]) the porous Si layer 110A remaining after the splitting process is **removed by etching**. Since Matushiita, et al. specifically discloses removing the remaining porous Si layer 110A from their structure, the prior art structure does not include a residual porous layer, as presently claimed. Applicants observe that in the various other embodiments disclosed in Matushiita, et al. the porous Si layer is also removed from the structure.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the claimed invention, as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Matushiita, et al. Applicants respectfully submit that the instant § 102 rejection has been obviated and withdrawal thereof is respectfully requested.

Turning to the various § 103 rejections, applicants respectfully submit that the combined disclosures of Matushiita, et al. and Sakaguchi, et al. or Mizuno do not render the claimed structure unpatentable. Specifically, none of the applied references teach or suggest the claimed structure including the elements now recited in Claim 31. That is, the suggested combination of prior art references does not teach or suggest a structure in which a residual porous layer remains.

The principal reference spurring each of the obviousness rejections, i.e., Matushiita, et al., is defective for the reasons mentioned above in regard to the anticipation rejection. Thus, those remarks are incorporated herein by reference. To reiterate: Matushiita, et al. do not teach or suggest an integrated circuit structure that includes a residual porous layer therein. Instead, Matushiita, et al. remove, via etching, the remaining porous Si layer from their structure. Thus, Matushiita, et al. teach directly away from the claimed structure.

Sakaguchi, et al., which provide a process for producing a semiconductor article that can be suitably used for producing a semiconductor devices such as a semiconductor integrated circuit, a solar cell, a semiconductor laser device or a light emitting diode, do not alleviate the above defects in Matushitta, et al. Specifically and in broad terms, Sakaguchi, et al. disclose using a film such as an adhesive film as a means for removing a porous Si layer from a substrate. Any remaining porous Si left on the substrate is disclosed as being "selectively removed on the basis that the porous Si layer has a low mechanical strength and a large surface area". See, for example, Col. 13, lines 15-25. The various embodiments provided in the Sakaguchi, et al. disclosure do not teach or suggest the claimed structure. In particular, the applied reference does not teach or suggest a structure that includes a semiconductor layer that includes a residual porous layer. In Sakaguchi, et al., and as mentioned above, the remaining porous Si layer is removed after the layer transfer process.

As such, applicants' claimed structure is not rendered unpatentable by the disclosures of Matushiita, et al. and Sakaguchi, et al.

Mizuno, which provides a thin film semiconductor device capable of improving the optical absorption efficiency of a single crystal silicon thin film solar battery, does not

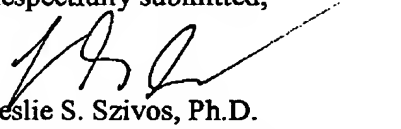
alleviate the above defect in Matushiita, et al. since the applied secondary reference also does not teach or suggest the presence of a residual porous layer. Instead, during the process disclosed in Mizuno a portion of the porous Si layer that remains after the splitting step is an insulation layer 22A that is formed by hydrogen annealing. The hydrogen anneal fills the pores at the surface of porous Si layer 22. See Col. 5, lines 16-20. As such, the disclosure of Mizuno teaches and suggests that a hydrogen anneal is used to form an insulation layer 22A having filled pores in the porous Si layer and that after the splitting process the insulation layer 22A having filled pores remains. In the present invention, a residual porous layer remains, not an insulation layer in which the pores have been filled as is the case with the disclosure of Mizuno.

The § 103 rejections also fail because there is no motivation in the prior art that suggests modifying the disclosed structure to include the features recited in Claim 31. Thus, there is no motivation provided in the applied reference, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Wherefore, consideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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